In the Specification:

Amend the first paragraph of the application, on Page 1, as follows:

This application is a continuation-in-part of the inventors' prior application Serial No. 09/575,488, filed May 19, 2000, entitled Method for Testing Circuits, now U.S. Patent No. 6,865,500, issued March 8, 2005, and claims the benefit of the provisional application Serial No. 60/197,749, filed April 18, 2000, entitled ATPG for Prediction of Analog Specifications, and Serial No. 60/203,602, filed May 12, 2000, entitled Test Generation for High Frequency and RF Circuits, each incorporated by reference in their entireties herein.

Amend the first paragraph under the heading "Detailed Description of a Preferred Embodiment" on Page 4 of the application as indicated below:

The present application incorporates herein by reference ~~in its entirety the publication by inventors R. Voorakaranam and A. Chatterjee~~ that portion of the U.S. provisional application Serial No. 60/197,749, now expired, entitled "Test Generation for Accurate Prediction of Analog Specifications," ~~IEEE VLSI Test Symposium, pp. 137-142, 2000. This publication~~ which provides mathematical explanation, background and support for methods according to the invention that are described herein in a simplified manner. Also incorporated herein is the inventor's paper, submitted to the International Test Conference 2001, entitled "Low-Cost Signature Testing of RF Circuits," attached hereto as Appendix A.

Amend the paragraph relating to the description of Figure 6 under the heading "Brief Description of the Drawings" on Page 4 as indicated below:

Figure 6 is a ~~flow chart of~~ block diagram illustrating a preferred method for low cost signature testing of RF electric circuits according to the present invention.

Amend the first full paragraph on Page 6 as indicated below:

In step 113, "g" is iterated in steps 110 and 112, i.e., these steps are carried out with respect to circuits C(2), C(3), . . . C(G). Accordingly, by the conclusion of step 113 for the initial stimulus Stim(k=0), each of the circuits C(g) has been stimulated with the stimulus Stim(0), corresponding signatures Sig(g,0,t) have been determined, and corresponding actual performance parameters $P_1(i)_A$, $P_2(i)_A$, . . . [[$P_G(Ii_A]]$ $P_G(Ii_A)$ have been measured.